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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/319,258	06/11/1999	MOTOO ASAI	P17856	2717

7055 7590 04/23/2003

GREENBLUM & BERNSTEIN, P.L.C.
1950 ROLAND CLARKE PLACE
RESTON, VA 20191

EXAMINER
ALCALA, JOSE H

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/23/2003 #23

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/319,258	Applicant(s) ASAI ET AL.	
	Examiner Jose H Alcala	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2002 and 04 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,22-27 and 44-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-8,11,12,27,46,47 and 49* is/are allowed.

6)☒ Claim(s) *1-5,9,10,22-26,44,45 and 48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-5,22-26,44 and 45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 fails to particularly point out and distinctly claim the structure of the invention and merely narrates the process of making the invention. For example see lines 2-4, where the claim merely recites the process of making the device, but fails to clearly claim the actual structure of the device. It is unclear, if the conductor circuit and the insulating substrate are already formed, how can they be: "repeating formation of conductor circuit and an interlaminar insulating layer". In addition, it is noted that those kinds of limitations are known as product by process limitations. If the product in the product-by-process claims are the same as or obvious from a product of the prior art, the claims are unpatentable even tough the prior product was made by a different process. See In re Thorpe, 227 USPQ 964,966 (Fed.Cir 1985). A "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173

USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Claim 2 fails to particularly point out and distinctly claim the structure of the invention and merely narrates the process of making the invention. For example see lines 2-4, where the claim merely recites the process of making the device, but fails to clearly claim the actual structure of the device. It is unclear, if the conductor circuit and the insulating substrate are already formed, how can they be: "repeating formation of conductor circuit and an interlaminar insulating layer". In addition, it is noted that those kinds of limitations are known as product by process limitations.

Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: what is the exact location of the roughened layer. Is the roughened layer located on the via-hole, or is the roughened layer located on "at least a part of the surface" of the conductor circuit. The

claim language of lines 5-7 is not clear on describing where on the board is the roughened layer, and if there are more than one roughened layers.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura (US Patent No. 5,517,758). As best understood by the examiner:

Regarding Claim 9, Nakamura teaches a multilayer printed circuit board (device of Figure 9B) comprising a substrate (reference number 91) provided with an under layer conductor circuit (reference number 93), an interlanminar insulating layer (reference number 94) formed thereon and an upper layer conductor circuit (top reference number 93) formed on the interlaminar insulating layer, a viahole (reference number 96) connecting both conductor circuits to each other and a roughened surface (reference number 98) plated on at least a part of the surface of the underlayer conductor circuit (reference number 93) connected to the viahole (reference number 96). Nakamura teaches a via hole (reference number 96), which is made by electroless plating and then electrolytic plating and roughened (column 9, lines 59-67, and column 10, lines 1-3). It is inherent then that the viahole inherently has an electroless plated film and an electrolytic plated film and a roughened layer having a roughened surface.

The limitations reciting that the roughened surface is formed by etching treatment, polishing treatment, or redox treatment are product by process limitations, and have not been given patentable weight.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1,3,4,44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (US Patent No. 5,517,758). As best understood by the examiner:

Regarding Claim 1, Nakamura teaches a multilayer printed circuit board (device of Figure 7F) comprising a plurality of interlaminar insulator layers (reference numbers 74) and conductor circuits (reference numbers 73), said printed circuit board being formed by laminating a first interlaminar insulating layer (reference number 74) on a conductor circuit (reference number 73) of a substrate (reference number 71) and repeating formation of conductor circuit (reference number 73) and an interlaminar insulating layer (reference number 74) on the other side of the substrate and a roughened layer (reference number 77, same as reference number 4) on at least a part of the surface of the conductor circuit, but fails to explicitly teach that the conductor circuit of reference number 74 is comprised of an electronics plated film and an electrolytic plated film.

Nakamura teaches a conductor circuit (reference number 88), which is made by electroless plating and then electrolytic plating (column 9,lines 25-27), the conductor circuit inherently has an electroless plated film and an electrolytic plated film. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Nakamura in order to have the conductor circuit made comprising an electroless plated film and an electrolytic plated film, thus increasing the density of the printed circuit board.

Regarding claim 3, Nakamura fails to explicitly teach that the roughened layer (reference number 77) is on at least a part of the surface inclusive of a side surface of the conductor circuit (reference number 73). Nakamura teaches the roughened layer on a top face of the conductor circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Nakamura in order to have the roughened layer on at least a part of the surface inclusive of a side surface of the conductor circuit, thus increasing the contact area between the two and improving conductivity.

Regarding claim 4, Nakamura fails to explicitly teach that the roughened layer (reference number 77) is on at least a part a side face of the conductor circuit (reference number 73). Nakamura teaches the roughened layer on a top face of the conductor circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Nakamura in order to have the roughened layer on at least a part of the side face of the conductor circuit, thus increasing the contact area between the two and improving conductivity.

Regarding Claims 5,25 and 26, Nakamura fails to explicitly teach that the roughened layer is a plated layer of copper-nickel-phosphorous alloy. It is well known in the art to coat conductors with alloys of copper, nickel and other elements, to improve conduction and reduce oxidation of conductors. It would have been obvious to one having ordinary skill in the art at the time the invention was made to coat the conductors with alloys of copper, nickel and other elements in order to improve conduction and reduce oxidation of conductors. In addition, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding Claim 44, Nakamura as modified supra for claim 1, inherently teaches that the electrolytic plated film is formed on the electronics plated film (column 9,lines 25-27).

8. Claims 2,22-24, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (US Patent No. 5,517,758) in view of Adlam et al. (US Patent No. 5,861,076). As best understood by the examiner:

Regarding Claim 2, Nakamura teaches a multilayer printed circuit board (device of Figure 7F) comprising a plurality of interlaminar insulator layers (reference numbers 74) and conductor circuits (reference numbers 73), said printed circuit board being formed by laminating a first interlaminar insulating layer (reference number 74) on a conductor circuit (reference number 73) of a substrate (reference number 71) and repeating formation of conductor circuit (reference number 73) and an interlaminar

insulating layer (reference number 74) on the other side of the substrate and a roughened layer (reference number 77, same as reference number 4) on at least a part of the surface of the conductor circuit, but fails to explicitly teach that the conductor circuit of reference number 74 is comprised of an electronics plated film and an electrolytic plated film, and fails to teach that the surface of the roughened layer is covered with a layer of a metal having an ionization tendency of more than copper but not higher than titanium, or of a noble metal.

Nakamura teaches a conductor circuit (reference number 88), which is made by electroless plating and then electrolytic plating (column 9,lines 25-27), the conductor circuit inherently has an electroless plated film and an electrolytic plated film. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Nakamura in order to have the conductor circuit made comprising an electroless plated film and an electrolytic plated film, thus increasing the density of the printed circuit board.

Furthermore, Adlam teaches that the surface of the roughened layer is covered with a layer of a metal having an ionization tendency of more than copper but not higher than titanium, or of a noble metal (Column 10, lines 11-29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Nakamura and Adlam, in order to have the surface of the roughened layer is covered with a layer of a metal having an ionization tendency of more than copper but not higher than titanium, or of a noble metal, thus providing passivation properties to the device.

Regarding claim 22, Nakamura as modified by Adlam, fails to explicitly teach that the roughened layer (reference number 77) is on at least a part of the surface inclusive of a side surface of the conductor circuit (reference number 73). Nakamura teaches the roughened layer on a top face of the conductor circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Nakamura in order to have the roughened layer on at least a part of the surface inclusive of a side surface of the conductor circuit, thus increasing the contact area between the two and improving conductivity.

Regarding claim 23, Nakamura as modified by Adlam, fails to explicitly teach that the roughened layer (reference number 77) is on at least a part a side face of the conductor circuit (reference number 73). Nakamura teaches the roughened layer on a top face of the conductor circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Nakamura in order to have the roughened layer on at least a part of the side face of the conductor circuit, thus increasing the contact area between the two and improving conductivity.

Regarding Claim 24, Nakamura as modified by Adlam, fails to explicitly teach that the roughened layer is a plated layer of copper-nickel-phosphorous alloy. It is well known in the art to coat conductors with alloys of copper, nickel and other elements, to improve conduction and reduce oxidation of conductors. It would have been obvious to one having ordinary skill in the art at the time the invention was made to coat the conductors with alloys of copper, nickel and other elements in order to improve conduction and reduce oxidation of conductors. In addition, it has been held to be within

the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding Claim 45, Nakamura as modified by Adlam, inherently teaches that the electrolytic plated film is formed on the electronics plated film (column 9,lines 25-27 of Nakamura).

9. Claims 10,and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (US Patent No. 5,517,758). As best understood by the examiner:

Regarding Claim 24, Nakamura as stated supra for claim 9, fails to explicitly teach that the roughened layer is a plated layer of copper-nickel-phosphorous alloy. It is well known in the art to coat conductors with alloys of copper, nickel and other elements, to improve conduction and reduce oxidation of conductors. It would have been obvious to one having ordinary skill in the art at the time the invention was made to coat the conductors with alloys of copper, nickel and other elements in order to improve conduction and reduce oxidation of conductors. In addition, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding Claim 48, Nakamura as stated supra for claim 9, inherently teaches that the electrolytic plated film is formed on the electronics plated film (column 9, lines 59-67, and column 10, lines 1-3)).

Allowable Subject Matter

10. Claims 6-8,11,12,27,46,47,49 are allowed.

Response to Arguments

11. Applicant's arguments with respect to claims 1-5,9,10,22-26,44,45,48 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references teach some of the elements of the instant claimed invention: Weglin (US Patent No. 4,017,968), Inaba et al. (US Patent No. 5,369,881), Tanaka et al. (US Patent No. 5,260,518), Angele et al. (US Patent No. 3,612,743), Knudsen et al. (US Patent No. 5,322,976), Lemke (US Patent No. 3,996,416), Russell et al. (US Patent No. 5,993,945), Farnworth et al. (US Patent No. 5,495,667) and Enomoto (US Patent No. 4,715,117).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA
April 20, 2003

DAVID L. TALBOTT
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800